REMARKS

Applicants respectfully request that the Claims in the above-identified patent application be reconsidered and again examined in view of the following remarks.

Applicant respectfully requests that the correction to the drawings as submitted to the Chief Draftsman be approved. Applicant has corrected Figures 1 and 2 by designating the figures as Prior Art as shown in red on the enclosed copies.

Claims 1-18 are pending. Claims 1, 3-6, 11, and 16-18 were allowed. Claims 5 and 11 were amended to correct typographical errors. Claims 2, 7-10, 12, and 14-15 were amended. No new matter was added.

The Examiner rejected Claims 2, 7-10, and 12-15 under 35 U.S.C. 103(a) as being as being unpatentable over Whetsel (US 6,262,587).

Amended Claim 2 recites: "portions of the electrical conductor spanning the regions in the fractional portion of the wafer, such conductor elevated above the regions in the fractional portion of the wafer." Whetsel discloses electrical conductors which are integral to the wafer. Applicants' electrical conductor is provided separate from the wafer and is thus elevated above the regions in the fractional portion of the wafer. Independent Claim 2 is patentably distinct over Whetsel since Whetsel neither describes nor suggests a conductor elevated above the regions in the fractional portion of the wafer.

Amended Claims 10 and 12 recite: "such conductor elevated above the regions in the fractional portion of the wafer." Claim 10 is patentably distinct over Whetsel for reasons analogous to those above in conjunction with Claim 2.

Amended Claim 7 recites: "a fusible link disposed in the one of the memory array regions electrically connecting the electrical interconnect and the periphery electrical component." Applicant respectfully submits that Whetsel neither describes nor suggests a fusible link disposed in the one of the memory array regions as recited in Claim 7.

Amended Claim 15 recites: "a fusible link disposed in the one of the memory array regions." Claim 15 is patentably distinct over Whetsel for reasons analogous to those above in conjunction with Claim 7.

Amended Claim 8 recites: "a fusible link disposed in one of the plurality of integrated circuit chips and electrically connecting the electrical interconnect and the periphery electrical component." Applicant respectfully submits that Whetsel neither describes nor suggests a fusible link disposed in the one of the plurality of integrated circuit chips as recited in Claim 8.

Amended Claim 9 recites: "an electrical interconnect for electrically connecting the array region of the one of the chips to the periphery electrical component, such electrical interconnect elevated above one of the separating regions." Whetsel discloses electrical conductors which are integral to the wafer. Applicants' electrical conductor is provided separate from the wafer and is thus elevated above one of the separating regions. Independent Claim 9 is patentably distinct over Whetsel since Whetsel neither describes nor suggests a conductor elevated above one of the separating regions.

Amended Claim 14 recites: "such electrical interconnect elevated above one of the separating regions." Claim 14 is patentably distinct over Whetsel for reasons analogous to those above in conjunction with Claim 9.

Applicant submits that all of the claims are now in condition for allowance, which action is requested.

Authorization to charge Daly, Crowley & Mofford, LLP Deposit Account No. 50-0845 for any excess fees due or credit any overpayment is hereby given.

Respectfully submitted,

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Barry Gaiman
Registration No. 42,562
Attorney for the Applicant(s)
Daly, Crowley & Mofford, LLP
275 Turnpike Street - Suite 101
Canton, MA 02021-2310
Telephone: (781) 401-9988 ext. 22
Facsimile : (781) 401-9966

Attachment: 4 Sheets of Claims with markings showing changes made, copy of letter to Chief Draftsman.

Version of the Claims with Markings to Show Changes Made

2. (Amended) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

an electrical conductor electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer, such conductor elevated above the regions in the fractional portion of the wafer.

5. (Amended) The method recited in claim 4 including configuring electrical functionality of the assembly comprising:

selectively cutting the electrical conductor on the dielectric member and fusing selected regions of an interconnecting bus on the chips.

7. (Amended) A semiconductor memory, comprising:

(A) a fractional portion of a semiconductor wafer, such fractional portion having:

a plurality of integrated circuit chips, each one of such chips comprising:

a memory array region;

wherein the chips have separating regions therebetween;

a periphery electrical component disposed in one of the separating regions;

(B) an electrical interconnect for electrically connecting the array region of one of the chips to the periphery electrical component; and

(C) a fusible link disposed in the one of the memory array regions electrically connecting the electrical interconnect and the periphery electrical component.

8. A semiconductor memory, comprising:

(A) a fractional portion of a semiconductor wafer, such fractional portion having:

a plurality of integrated circuit chips, each one of such chips comprising:

a memory array region;

wherein the chips have separating regions therebetween;

a periphery electrical component disposed in one of the chips;

(B) an electrical interconnect for electrically connecting the array region of one of the chips to the periphery electrical component; and

(C) a fusible link disposed in one of the plurality of integrated circuit chips and electrically connecting the electrical interconnect and the periphery electrical component.

9. A semiconductor memory package, comprising:

(A) a fractional portion of a semiconductor wafer, such fractional portion having:

a plurality of integrated circuit chips, each one of such chips comprising:

a memory array region; and

wherein the chips have separating regions therebetween;

a periphery electrical component disposed in one of the separating regions;

(B) an electrical interconnect for electrically connecting the array region of the one of the chips to the periphery electrical component, such electrical interconnect elevated above the one of the separating regions.

10. (Amended) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips having separating regions between them, the fractional portion of the wafer having a plurality of electrical contacts electrically connected to the chips;

an electrical conductor electrically connected to the plurality of electrical contacts to electrically interconnect such chips with portions of the electrical conductor spanning the separating regions between the chips in the fractional portion of the wafer, such conductor

elevated above the regions in the fractional portion of the wafer.

11. (Amended) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions between them; such fractional portion of the wafer having a plurality of electrical contacts electrically connected to the chips;

a dielectric having an electrical conductor thereon, such electrical conductor electrically connecting the plurality of electrical contacts to electrically interconnect ~~of~~ such chips with portions of the electrical conductor spanning the separating regions between the chips in the fractional portion of the wafer.

12. (Amended) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having:

a plurality of integrated circuit chips thereon, such chips have separating regions between them;

electrical components;

an electrical conductor ~~to~~ for electrically connecting the plurality of electrical contacts to electrically interconnect such chips with the electrical components, such conductor elevated above the separating regions in the fractional portion of the wafer.

14. A semiconductor memory, comprising:

a fractional portion of a semiconductor wafer, such fractional portion of the wafer comprising:

a plurality of integrated circuit chips, each one of such chips having a memory array region;

separating regions between the chips;

a periphery electrical component disposed in one of the separating regions

an electrical interconnect for electrically connecting the chip to the periphery

electrical component, such electrical interconnect elevated above one of the separating regions in the fractional portion of the wafer.

15. A semiconductor memory, comprising:

a fractional portion of a semiconductor wafer, such fractional portion of the wafer comprising:

a plurality of integrated circuit chips, each one of such chips having a memory array region, the chips have separating regions therebetween;

a peripheral electrical component disposed the one of the separating regions;

an electrical interconnect for electrically connecting the chip to the peripheral electrical component; and

a fusible link disposed in the one of the memory array regions and electrically connecting the electrical interconnect and the periphery electrical component.